CLAIMS

What is claimed is:

1. An instruction memory comprising:

memory locations, directly instruction-word-addressable, to store linear sequences of instruction data in logically contiguous memory locations of increasing logical word address, including instructions that are one or multiple instruction words in size, wherein instructions stored in the memory locations may be fetched in a single instruction cycle;

memory control logic to indicate a current valid read word address of the memory locations; and

a permutation unit to receive instruction data read from the memory locations and order the instruction data according to an order of sequential operation.

2. An instruction memory according to claim 1, wherein the memory locations are byte addressable.

3. An instruction memory according to claim 1, wherein the memory locations are two-byte addressable.

4. An instruction memory according to claim 1, wherein the memory locations further comprise multiple banks of addressable locations, each bank having multiple directly addressable lines of instruction data.

5. An instruction memory according to claim 4, wherein each bank is one instruction word in width.

6. An instruction memory according to claim 1, wherein the memory control logic further comprises a pair of memory location pointers to define a window of valid instruction data.

7. An instruction memory according to claim 6, wherein a read request outside the window of valid instruction data causes the memory control logic to set the pair of pointers equal to each other to invalidate the data in the memory locations.

8. An instruction memory according to claim 7, further comprising determining if the read request outside the window of valid instruction data jump is a forward jump to an instruction address whose address offset from the current instruction address is less than a threshold, and if the address offset is less than the threshold, continuing to fetch instructions until the instruction of the forward jump has been fetched.

9. A memory structure for storing variable-instruction-size instructions comprising:

multiple rows of word-addressable instruction data memory locations, the rows of memory locations to receive instruction data in lexical order from a system level-1 (L1) cache and store the instruction data in lexical order in the rows of memory locations, wherein the instruction data is retrievable in a single instruction clock cycle; and

control logic coupled with the rows of memory locations, to provide control signals to cause reading and writing of memory locations, and to order the instruction data read from the memory locations in lexical execution order.

10. A memory structure according to claim 9, wherein the rows of memory location to store the instruction data in lexical order further comprises storing logically separable units of instruction data in sequential memory locations spanning multiple rows.

11. A memory structure according to claim 9, wherein the control logic further comprises address indicators to indicate at least a top and a bottom of a window of valid instruction data.

12. A memory structure according to claim 11, wherein the address indicators comprise an address indicator to indicate the top instruction of a loop and an address indicator to indicate the bottom instruction of a loop.

13. A memory structure according to claim 9, wherein the memory locations to store instruction data comprises the memory locations to store at least the first instructions of a software loop, and the control logic to provide control signals comprises the control logic to provide control signals to cause the reading and execution of the stored first instructions of the software loop as a zero-overhead loop buffer.

14. An electronic system comprising:

a processor having a sequencer coupled to a level-zero cache to store variable-instruction-size instructions, the level zero (L0) cache including instruction-word addressable memory locations to store a series of instruction data in execution order, each instruction of the series of instruction data retrievable in a single instruction clock cycle, the L0 cache having read and write logic to write the instruction data to the memory locations, read the data from the written memory locations, and align the data in execution order; and

a power storage cell coupled with the processor to provide power to the processor.

15. A system according to claim 14, wherein the memory locations are byte addressable.

16. A system according to claim 14, wherein the memory locations are two-byte addressable.

17. A system according to claim 14, wherein the memory locations further comprise multiple banks of addressable locations, each bank having multiple directly addressable lines of instruction data.

18. A system according to claim 17, wherein each bank is one instruction word in width.

19. A system according to claim 14, wherein the read logic further comprises memory location pointers to define a window of valid instruction data.

20. A system according to claim 19, wherein a read request for a memory location outside the window of valid instruction data causes the processor to fetch more instruction data to alter the window of valid instruction data until the requested memory location is within the window.

21. A method comprising:

storing units of instruction data in logically sequential memory locations of a level-0 (L0) storage structure;

indicating a top-most valid instruction data unit, a bottom-most valid instruction data unit, and a current instruction data unit to execute with pointers;

reading a number of instruction data units from the L0 storage structure, starting at the memory location of the current instruction data unit pointer; and

rearranging the read instruction data units to align the instruction data units in preparation for execution of an instruction.

22. A method according to claim 21, wherein the instruction data unit comprises a number of bits equal to the number of bits in a smallest instruction size supported in a processor that supports variable instruction sizes.

23. A method according to claim 21, wherein reading the number of instruction data units comprises reading a number of instruction data units equal to a maximum number of instruction data units that an instruction latch in a processor instruction sequencer can hold simultaneously.

24. A method according to claim 23, wherein reading from the memory location of the current instruction data unit comprises reading the number of instruction data units starting from a memory location in the center of a row of memory locations, and reading the instruction data

units stored in all memory locations in the row from the location in the center to the last memory location in the row, and reading at least one instruction data unit from a memory location in the next row.

25. A method according to claim 24, wherein rearranging comprises shifting the read instruction data units to order the instruction data units with the current instruction data unit to occupy the least significant bytes of the sequencer.